AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method for producing a transistor structure ~~structures~~ with a lightly doped drain (LDD), ~~in which~~ the method comprising:

structuring a gate electrode ~~(3) is structured~~ on a gate dielectric ~~(2)~~, the gate dielectric being on ~~an essentially~~ a substantially planar upper surface of a semiconductor body or substrate; ~~(1), and~~

~~using the gate electrode (3) as a mask, implantations of dopant are performed for the purpose of creating source/drain regions (12) and regions (11) of lower dopant concentration that are adjacent to the former on the channel side, characterized in that~~

~~after the structuring of the gate electrode (3)~~ etching the semiconductor body or substrate ~~(1) is etched such that on the source side and on the drain side~~ to form sloping sidewalls on regions ~~(5) are formed~~ adjacent to the gate electrode, the sloping sidewalls ~~(3) and~~ sloping downward ~~toward the outside~~ from the gate electrode; ~~(3),~~

depositing a spacer layer over at least part of the sloping sidewalls and the gate electrode; ~~(6) is deposited, conforming with the edges,~~

~~which is then~~ anisotropically ~~back-etched~~ back-etching the spacer layer to form spacers ~~(7)~~, ~~which at least partially cover~~ the spacers at least partially covering source-side and drain-side sidewalls of the gate electrode ~~(3)~~ and the sloping sidewalls; ~~(5),~~

using the gate electrode ~~(3)~~ as a mask, ~~implantations of~~ implanting dopant ~~are performed for the purpose of creating source/drain regions (12)~~ in the semiconductor body or substrate to form a source region, a drain region, and regions ~~(11)~~ of lower dopant concentration, the regions of lower dopant concentration being adjacent to the source and drain regions and adjacent to a channel between the source and drain regions; ~~former on the channel side~~

~~and the implantation of~~ wherein implanting dopant is performed at a ~~high~~ first angle relative to the ~~original~~ upper surface of the semiconductor body or substrate to form the source and drain regions; and

~~(12) and~~ wherein implanting dopant is performed at a ~~low~~ second angle relative to the ~~original~~ upper surface of the semiconductor body or substrate, and through the spacers ~~(7)~~, to form the regions ~~(11)~~ of lower dopant concentration, the first angle being greater than the second angle.

2. (Currently Amended) The method ~~according to~~ of claim 1, ~~in which~~ wherein the sloping sidewalls ~~(5)~~ are formed at ~~a slope angle~~ angles of 30° to 60° from the ~~original~~ upper surface of the semiconductor body or substrate ~~(1)~~.

3. (Currently Amended) The method ~~according to~~ of claim 2, ~~in which~~ wherein the sloping sidewalls ~~(5)~~ are formed at ~~a slope angle~~ angles of 45° from the ~~original~~ upper surface of the semiconductor body or substrate ~~(1)~~.

4. (Currently Amended) The method of claim 1 ~~according to one of claims 1 through 3, in which the implantation for the purpose of forming~~ wherein implanting to form the regions ~~(11)~~ of lower dopant concentration is performed in a direction that, ~~in an intersecting plane that is oriented vertically on the upper surface of the substrate (1) and the sloping sidewalls (5),~~ forms an angle of between 30° and 60° with a surface normal ~~on~~ to the ~~original~~ upper surface of the semiconductor body or substrate ~~(1)~~.

5. (Currently Amended) The method of claim 1 ~~according to one of claims 1 through 4, in which the implantation for the purpose of forming~~ wherein implanting to form the source and drain regions ~~(12)~~ is performed in a direction that, ~~in an intersecting plane that is oriented vertically on the upper surface of the substrate (1) and the sloping sidewalls (5),~~ forms an angle of between 0° and 7° with a surface normal to ~~on~~ the ~~original~~ upper surface of the semiconductor body or substrate ~~(1)~~.

6. (Currently Amended) The method of claim 1 ~~according to one of claims 1 through 5, in which, in the~~ wherein etching ~~of the sloping sidewalls (5),~~ comprises etching at least some of the semiconductor body or the substrate ~~(1) is also etched away somewhat~~ underneath the gate electrode ~~(3)~~.

7. (Currently Amended) The method of claim 1 ~~according to one of claims 1 through 6, in which with the~~ wherein etching ~~of the sloping sidewalls (5) the upper surface~~

~~of the substrate (1) is lowered by a depth (d), which ranges~~ comprises removing between ~~from~~ 20nm ~~to~~ and 200nm of the semiconductor body or the substrate.

8. (New) The method of claim 2, wherein implanting to form the regions of lower dopant concentration is performed in a direction that forms an angle of between 30° and 60° with a surface normal to the upper surface of the semiconductor body or substrate.

9. (New) The method of claim 2, wherein implanting to form the source and drain regions is performed in a direction that forms an angle of between 0° and 7° with a surface normal to the upper surface of the semiconductor body or substrate.

10. (New) The method of claim 2, wherein etching comprises etching at least some of the semiconductor body or the substrate underneath the gate electrode.

11. (New) The method of claim 2, wherein etching comprises removing between 20nm and 200nm of the semiconductor body or the substrate.

12. (New) The method of claim 4, wherein implanting to form the source and drain regions is performed in a direction that forms an angle of between 0° and 7° with a surface normal to the upper surface of the semiconductor body or substrate.

13. (New) The method of claim 12, wherein etching comprises etching at least some of the semiconductor body or the substrate underneath the gate electrode.

14. (New) The method of claim 12, wherein etching comprises removing between 20nm and 200nm of the semiconductor body or the substrate.

15. (New) The method of claim 1, wherein a sloping sidewall on the source-side and a sloping sidewall on the drain side slope downward from the gate electrode at substantially same angles.

16. (New) A method for producing a device structure, comprising:

forming a gate electrode on a gate dielectric, the gate dielectric being on an upper surface of a semiconductor;

removing at least part of the semiconductor to form sloping sidewalls adjacent to the gate electrode, the sloping sidewalls sloping downward relative to the gate electrode;

forming spacers at sides of the gate electrode and adjacent to the sloping sidewalls;

implanting dopant at a first angle relative to the upper surface of the semiconductor to form source and drain regions in the semiconductor; and

implanting dopant at a second angle relative to the upper surface of the semiconductor, and through the spacers, to form regions of lower dopant concentration in the semiconductor, the regions of lower dopant concentration being adjacent to a channel between the source and drain regions;

wherein the first angle is greater than the second angle.

17. (New) The method of claim 16, wherein the sloping sidewalls are formed at angles of 30° to 60° from the upper surface of the semiconductor.

18. (New) The method of claim 17, wherein the sloping sidewalls are formed at angles of 45° from the upper surface of the semiconductor.

19. (New) The method of claim 16, wherein implanting to form the regions of lower dopant concentration is performed in a direction that forms an angle of between 30° and 60° with a surface normal to the upper surface of the semiconductor.

20. (New) The method of claim 16, wherein implanting to form the source and drain regions is performed in a direction that forms an angle of between 0° and 7° with a surface normal to the upper surface of the semiconductor.